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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/804,945	03/19/2004	Curtis R. Priem	NVDA P000455	9182

26291 7590 11/23/2011

PATTERSON & SHERIDAN L.L.P. NJ Office
3040 Post Oak Boulevard
Suite 1500
Houston, TX 77056-6582

EXAMINER	
CLEARY, THOMAS J	

ART UNIT	PAPER NUMBER
2111	

MAIL DATE	DELIVERY MODE
11/23/2011	PAPER

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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte CURTIS R. PRIEM

Appeal 2009-010861
Application 10/804,945
Technology Center 2100

Before: JEAN R. HOMERE, JOHN A. JEFFERY, and
ST. JOHN COURTENAY III, *Administrative Patent Judges*.

COURTENAY, *Administrative Patent Judge*.

DECISION ON APPEAL

Appellant appeals under 35 U.S.C. § 134(a) from a final rejection of claims 1-15, 17, 18, and 21-23. Claims 16, 19, and 20 were cancelled during prosecution. We have jurisdiction under 35 U.S.C. § 6(b).

We Affirm-in-part.

STATEMENT OF THE CASE

Introduction

Appellant's invention relates to a method and apparatus for scheduling threads. More particularly, the invention on appeal is directed to providing a method that schedules threads based on latency. (Spec. 1.).

Exemplary Claim

Claim 1 is an exemplary claim and is reproduced below:

1. Method for scheduling the service of a thread, said method comprising the steps of:

masking interrupts from hardware devices in order to ignore interrupts for other threads;

acquiring a latency information associated with the thread, wherein the latency information indicates a time at which the thread needs to be processed;

unmasking interrupts from the hardware devices in order to detect interrupts for the other threads; and

rearranging an order in which the thread and the other threads will be serviced in a single queue to schedule the thread for processing in accordance with said latency information, wherein the rearranging is performed simultaneously for the thread and the other threads, and the thread and the other threads that are ordered in the single queue correspond to all requests received from the hardware devices.

Rejections

1. Claims 1, 3, 4, 9, 10, and 23 stand rejected under 35 U.S.C. §103(a) as being unpatentable over the combination of Zolnowsky (U.S. Pat. No.

5,826,081), Browning (U.S. Pat. No. 6,633,897 B1), and Jones (U.S. Pat. No. 5,812,844).

2. Claims 1-15, 17, 18, and 23 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over the combination of Ramakrishnan (U.S. Pat. No. 6,085,215), Jones, and knowledge commonly known in the art, as evidenced by Browning. (*See* Ans. 2-3).

3. Claims 21 and 22 stand rejected under 35 U.S.C. §103(a) as being unpatentable over the combination of Ramakrishnan, Jones, Browning, and Cheng (U.S. Pat. Pub. No. 2002/0083143 A1).

ANALYSIS

First-stated § 103 rejection

We begin our analysis by reviewing the Examiner's first-stated rejection of claims 1, 3, 4, 9, 10, and 23 as being unpatentable over the combination of Zolnowsky, Browning, and Jones.

Appellant contends that the cited combination of references fails to teach or suggest the following limitations recited in commensurate form in independent claims 1 and 9: (i) masking interrupts from hardware devices, (ii) unmasking interrupts from the hardware devices, (iii) simultaneously rearranging threads in a single queue, and (iv) ordering all requests from the hardware devices in the single queue. (App. Br. 10).

Based upon our review of the administrative record, we have determined that the following issue is dispositive regarding the first-stated rejection:

Issue: Under §103, did the Examiner err by finding that the combination of Zolnowsky, Browning, and Jones would have taught or suggested masking interrupts and unmasking interrupts from the hardware devices, within the meaning of independent claims 1 and 9?

Based upon our review of the record, we agree with Appellant that Zolnowsky fails to teach or fairly suggest the limitations of masking and unmasking interrupts from hardware devices. (App. Br. 10, last paragraph).

In the rejection of claim 1, the Examiner finds these limitations are described in col. 6, lines 34-42 of Zolnowsky, where scheduling locks are described. (Ans. 4). We agree with the Examiner's claim construction in the "Response to Arguments:" "that the broadest reasonable interpretation of masking and unmasking interrupts is blocking interrupts from being sent to a processor (masking) and allowing interrupts to be sent to a processor (unmasking)." (Ans. 14). However, we find the Examiner has not shown where such interrupt masking is taught or suggested in column 6 of Zolnowsky, as relied upon in the rejection. (Ans. 4).

In the "Response to Arguments" section of the Answer, the Examiner additionally points to Zolnowsky at column 8, lines 55-64. Although "interrupt threads" are disclosed at col. 8, l. 65, we agree with Appellant that Zolnowsky merely teaches that "[i]nterrupt threads are always given the highest priority" (col. 8, lines 63-64) and does not teach or fairly suggest interrupt masking/unmasking within the meaning of Appellant's independent claims 1 and 9. (App. Br. 11, first paragraph).

Because the Examiner has not established on this record that Browning or Jones overcomes the deficiencies of Zolnowsky, we reverse the Examiner's first-stated § 103 rejection of independent claims 1 and 9 over

the combination of Zolnowsky, Browning, and Jones. For the same reasons discussed above, we also reverse the rejection of associated dependent claims 3, 4, 10, and 23 that were rejected over the same combination of references.

Second-stated § 103 rejection

We next review the Examiner's second-stated § 103 rejection of claims 1-15, 17, 18, and 23 as being obvious over the combination of Ramakrishnan, Jones, and knowledge commonly known in the art, as evidenced by Browning. (*See* Ans. 2-3).

For this second-stated rejection, Appellant argues claims 1-15, 17, 18, and 23 as a group. We select representative claim 1 to decide the appeal for this group. *See* 37 C.F.R. § 41.37(c)(1)(vii).

Regarding the Ramakrishnan primary reference (replacing Zolnowsky in the combination discussed above), Appellant presents the following principal contentions:

> Ramakrishnan also fails to teach or suggest the limitations recited in claims 1 and 9 set forth above [referring to the first-stated rejection]. Nowhere does Ramakrishnan teach or suggest using a queue to store processing threads. Therefore, Ramakrishnan fails [to] teach or suggest the limitations of ordering all requests from all of the hardware devices in a single queue and that all of the threads are simultaneously rearranged in the single queue.

(App. Br. 12).

Based upon our review of the administrative record, we have determined that the following issue is dispositive regarding the second-stated rejection:

Issue: Under §103, did the Examiner err by finding that the combination of Ramakrishnan, Jones and Browning, would have taught or suggested masking interrupts and unmasking interrupts from the hardware devices, and ordering all requests from the hardware devices in a single queue, and that all of the threads are simultaneously rearranged in the single queue, within the meaning of representative claim 1?

For this second-stated rejection, we find the weight of the evidence supports the Examiner's underlying factual findings and ultimate legal conclusion of obviousness for representative claim 1.

Unlike the Zolnowsky reference discussed above, Ramakrishnan expressly teaches enabling (i.e., unmasking) and disabling (masking) interrupts in the context of a thread scheduling system. (Col. 4, ll. 41, 46, col. 5, l. 24; *see also* Ans. 6). We conclude that this teaching would have rendered obvious the disputed masking/unmasking interrupt limitations, which we agree were notoriously well known in the art at the time of Appellant's invention, as evidenced by Ramakrishnan.

Although Appellant additionally contends that "Ramakrishnan fails to teach or suggest the limitations of ordering all requests from all of the hardware devices in a single queue and that all of the threads are simultaneously rearranged in the single queue" (App. Br. 12), we observe that the Examiner's rejection is based on the *combination* of the Ramakrishnan, Jones, and Browning references.

Ramakrishnan must be read, not in isolation, but for what it fairly teaches in combination with the prior art as a whole. *See In re Merck & Co., Inc.*, 800 F.2d 1091, 1097 (Fed. Cir. 1986) (one cannot show

nonobviousness by attacking references individually where the rejections are based on combinations of references.).

Here, we agree with the Examiner's finding that "Browning clearly discloses the use of a single run/execution queue (See Column 1 Lines 54-56, Column 3 Lines 28-35, and Abstract)," referring to Browning's single global execution queue 40 as shown in Fig. 2. (Ans. 15). Thus, the record supports the Examiner's finding that "it [was] notoriously old and well known in the art to store threads for processing in a single queue, as evidenced by Browning (See Column 1 Line 22 - Column 2 Line 32)." (Ans. 7).

Regarding the remaining argued limitations, we agree with the Examiner's additional findings:

> Ramakrishnan further discloses the use of deadline latency information when scheduling the threads (See Column 10 Lines 48-64), but does not disclose rearranging an order in which the thread and the other threads will be serviced in a single queue to schedule the thread for processing in accordance with said latency information, wherein the rearranging is performed simultaneously for the thread and the other threads. Jones discloses the use of deadline scheduling in which the order in which threads are scheduled for execution is simultaneously rearranged based on the latency of the thread (See Column 3 Lines 1-26).

(Ans. 7).

Based upon our review of the record, we agree with and adopt the aforementioned underlying factual findings by the Examiner which, in our view, are sufficient to support the Examiner's ultimate legal conclusion of obviousness. Therefore, for essentially the same reasons articulated by the

Examiner in the Answer (Ans. 16-17), as discussed above, we sustain the obviousness rejection of representative claim 1 over the combination of Ramakrishnan, Jones, and knowledge commonly known in the art, as evidenced by Browning.

For the same reasons, we also sustain the Examiner's obviousness rejection of the associated claims 2-15, 17, 18, and 23 (not separately argued) as being obvious over the identical combination of Ramakrishnan, Jones, and knowledge commonly known in the art, as evidenced by Browning. *See* 37 C.F.R. § 41.37(c)(1)(vii).

Third-stated § 103 rejection

We next review the Examiner's third -stated §103 rejection of claims 21 and 22 as being obvious over the combination of Ramakrishnan, Jones, Browning, and Cheng.

Appellant admits that "[i]n paragraph [0068], Cheng explicitly teaches the creation of threads: 'one for handling device discovery, one for handling device description, and one for handling device presentation.'" (App. Br. 13, last paragraph). However, Appellant avers that "[t]here is no teaching or suggestion that a thread is created for interrupt processing [referring to claim 21]. Furthermore, there is no teaching or suggestion that interrupt identification numbers are associated with any of the threads [referring to claim 22]." (App. Br. 13-14).

We find Appellant's arguments unpersuasive regarding claim 21, given Appellant's admission regarding Cheng's clear teaching of creating of threads (*id.*), and given our discussion above of Ramakrishnan's teaching of the notoriously well known use of interrupts in the context of thread

scheduling. For these reasons, we sustain the Examiner's rejection of dependent claim 21 as being obvious over the combination of Ramakrishnan, Jones, Browning, and Cheng.

However, we agree with Appellant that the Examiner has not fully developed the record to demonstrate *inherency* [1] regarding the first and second interrupt identification numbers that are used in the manner recited in claim 22:

> creating an additional thread, wherein a first interrupt identification number is associated with the thread and a second interrupt identification number that is different than the first interrupt identification number is associated with the additional thread and the additional thread is created for use during processing of a second interrupt that the one of the hardware devices is configured to generate;

(Claim 22).

Therefore, for essentially the same reasons argued by Appellant (App. Br. 13-14), we reverse the Examiner's §103 rejection of claim 22 over the combination of Ramakrishnan, Jones, Browning, and Cheng.

New Arguments in Reply Brief

"[T]he reply brief [is not] an opportunity to make arguments that could have been made in the principal brief on appeal to rebut the Examiner's rejections, but were not." *Ex parte Borden*, 93 USPQ2d 1473, 1474 (BPAI 2010) (informative).

[1] "The inherent teaching of a prior art reference, a question of fact, arises both in the context of anticipation and obviousness." *In re Napier*, 55 F.3d 610, 613 (Fed. Cir. 1995) (affirmed 35 U.S.C. § 103 rejection based in part on an inherent disclosure in one of the references).

Therefore, we decline to consider the untimely "teaching away" argument that Appellant advances for the first time in the Reply Brief. (Reply Br. 2). We likewise decline to consider the untimely arguments for dependent claims 2 and 12-14 that Appellant advances for the first time in the Reply Brief. (Reply Br. 4). These arguments have not been made in response to any shift in the Examiner's position and could have been presented in the principal Brief.

DECISION

We affirm the Examiner's § 103 rejection of claims 1-15, 17, 18, and 23 over the combination of Ramakrishnan, Jones, and knowledge commonly known in the art, as evidenced by Browning.

We affirm the Examiner's § 103 rejection of claim 21 over the combination of Ramakrishnan, Jones, Browning, and Cheng.

We reverse the Examiner's § 103 rejection of claims 1, 3, 4, 9, 10, and 23 over the combination of Zolnowsky, Browning, and Jones.

We reverse the Examiner's § 103 rejection of claim 22 over the combination of Ramakrishnan, Jones, Browning, and Cheng.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a)(1)(iv) (2009).

ORDER

AFFIRMED-IN-PART

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